

PCT

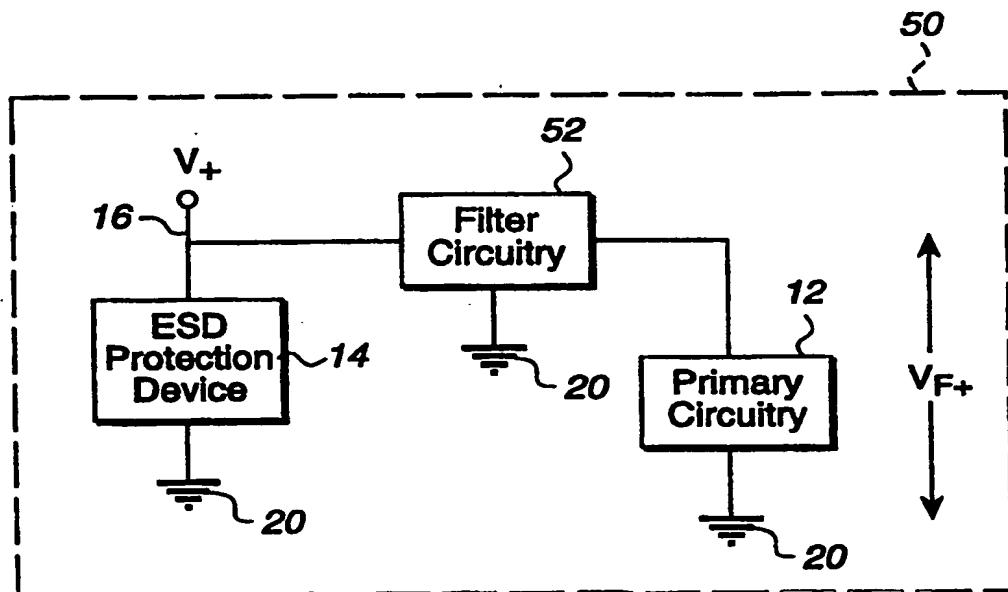
WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ :	A1	(11) International Publication Number:	WO 99/35742
H03K 5/08		(43) International Publication Date:	15 July 1999 (15.07.99)
(21) International Application Number:	PCT/US99/00420	(81) Designated States:	JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).
(22) International Filing Date:	8 January 1999 (08.01.99)		
(30) Priority Data:	9 January 1998 (09.01.98)	US	Published <i>With international search report.</i>
09/004,952			
(71) Applicant:	MAXIM INTEGRATED PRODUCTS, INC. [US/US]; 120 San Gabriel Drive, Sunnyvale, CA 94086 (US).		
(72) Inventor:	TANASE, Gabriel, E.; 10146 Amelia Court, Cupertino, CA 95014 (US).		
(74) Agent:	COLEMAN, Brian, R.; Hickman Stephens & Coleman, LLP, P.O. Box 52037, Palo Alto, CA 94303-0746 (US).		

(54) Title: FILTER CIRCUITS FOR PROTECTING AGAINST TRANSIENT ELECTRICAL PULSES



(57) Abstract

An integrated circuit package having primary circuitry, an ESD protection device (14), a filter circuit (102), and a conductive lead (16) arranged to couple a point (V_+) external to the integrated circuit package to a point (V_{F+}) internal to the integrated circuit package. The ESD device, coupled in series between the conductive lead and a ground reference (20), can limit the voltage magnitude of a transient electrical pulse occurring upon the conductive lead. The filter circuit is operable such that the voltage magnitude of an electrical signal generated at the filter circuit output (V_{F+}) is less than the voltage magnitude of the certain transient electrical pulse itself.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece	ML	Mali	TR	Turkey
BG	Bulgaria	HU	Hungary	MN	Mongolia	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MR	Mauritania	UA	Ukraine
BR	Brazil	IL	Israel	MW	Malawi	UG	Uganda
BY	Belarus	IS	Iceland	MX	Mexico	US	United States of America
CA	Canada	IT	Italy	NE	Niger	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NL	Netherlands	VN	Viet Nam
CG	Congo	KE	Kenya	NO	Norway	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NZ	New Zealand	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	PL	Poland		
CM	Cameroon	KR	Republic of Korea	PT	Portugal		
CN	China	KZ	Kazakhstan	RO	Romania		
CU	Cuba	LC	Saint Lucia	RU	Russian Federation		
CZ	Czech Republic	LI	Liechtenstein	SD	Sudan		
DE	Germany	LK	Sri Lanka	SE	Sweden		
DK	Denmark	LR	Liberia	SG	Singapore		
EE	Estonia						

FILTER CIRCUITS FOR PROTECTING AGAINST TRANSIENT
ELECTRICAL PULSES

Description

5 Technical Field

The present invention is related to filter circuits for protecting electrical devices from transient electrical pulses such as those caused by electrostatic discharge (ESD) events. More specifically, the present invention teaches coupling an ESD protection device together with a filter circuit in order to protect the primary electrical circuitry from ESD events which the ESD protection device does not adequately dissipate.

10 Background Art

15 Electrical devices of all types are susceptible to damage from transient electrical events. The short duration of transient electrical events such as electrostatic discharge (ESD) might make them appear innocuous. However, this is simply not the case.

20 Take, for example, the high susceptibility of many integrated circuits to ESD events. ESD, as will be appreciated, is the rapid discharge of static electricity from one conductor to another conductor having a different electrical potential. The typical integrated circuit includes a variety of conductors and electrical components that are generally intended to operate near the same potential. Hence, components internal to the integrated circuit are not designed to withstand the rapid discharge of electricity arising during ESD events. 25 However, when a lead of the integrated circuit comes into near contact with a conductor of a different potential (e.g., a human who has been walking over a carpet), an ESD event occurs potentially damaging the integrated circuit.

Figure 1 provides a schematic useful for describing how an ESD event may arise in connection with an integrated circuit 10 of the prior art. The integrated circuit 10 includes primary circuitry 12, an ESD protection device 14, and an input lead 16 coupled electrically to both the primary circuitry 12 and the ESD protection device 14. The primary circuitry 12 and the ESD protection device 14 are both coupled to a common ground reference 20. An impedance Z_1 models the effective impedance between the input lead 16 and an external conductor 30 that is the source of the static electricity.

When the external conductor 30 and the input lead 16 possess different potentials and are brought close enough together, the impedance Z_1 is such that an ESD event occurs. The ESD event generates a current I_{ESD} across the impedance Z_1 and a voltage V_{ESD} at the external conductor 30 with reference to the common ground 20. The typical ESD event lasts less than 300 nanoseconds, meaning that the energy has dissipated and both the voltage V_{ESD} and the current I_{ESD} are negligible after this time. However, while the ESD event is occurring, the voltage V_{ESD} and the corresponding I_{ESD} can be exceedingly high. For example, the voltage V_{ESD} from a normal human body discharge can exceed 3 kilo Volts.

Typical ESD protection devices such as ESD protection device 14 operate such that the resulting voltage V_+ across the primary circuitry 12 is less than 100 Volts with the bulk of the current I_{ESD} flowing through the ESD protection device 14 rather than the primary circuitry 12. For many integrated circuits, this reduction in applied voltage and the redirection of the current is sufficient protection to safeguard against any possible damage. However, certain integrated circuits are much more sensitive to transient electrical pulses and currently available ESD protection devices are not capable of providing the needed protection.

For example, certain integrated circuits include thin film fuses. These thin film fuses can be selectively blown, even after the integrated circuit has been packaged, in order to produce an integrated circuit having the desired electrical characteristics. This enables the electrical characteristics of the integrated circuit to be modified after the integrated circuit is fully packaged.

5 As will be appreciated, different selections of the fuses result in different electrical characteristics. These thin film fuses are sensitive to voltage spikes and may be inadvertently blown when an ESD event occurs, even when protected by a standard ESD protection device. Once a fuse is improperly blown, the electrical characteristics of the integrated circuit are irreversibly altered.

10

Accordingly, what is needed is a filter circuit that can work in conjunction with common ESD protection devices to provide enhanced protection from ESD events and other transient electrical events.

Disclosure of the Invention

In order to achieve the foregoing and in accordance with the present invention, a variety of filter circuits and integrated circuit packages are taught herein. A first filter circuit includes two resistors R₁ and R₂, two capacitors C₁ and C₂, and two transistors Q₁ and Q₂. These components are arranged such that transient voltage pulse applied at an input of the filter circuit is attenuated so that a voltage measured at the emitter of the transistor Q₁ (which is the output of the filter circuit) due to the transient voltage pulse is substantially less than the transient voltage pulse.

More specifically, the first terminals of resistors R₁ and R₂ and the collector of transistor Q₁ are electrically coupled and constitute the filter circuit input. The second terminal of the resistor R₂ and the first terminal of the capacitor C₂ are electrically coupled. The second terminal of the capacitor C₂ and the base of the transistor Q₂ are electrically coupled. The second terminal of the resistor R₁, the collector of the transistor Q₂, the first terminal of the capacitor C₁, and the base of the transistor Q₁ are electrically coupled. Finally, the emitter of the transistor Q₂ and the second terminal of the capacitor C₁ are electrically coupled.

In order to protect the transistor Q₂, another filter circuit of the present invention teaches coupling a resistor R₃ between the base of the transistor Q₂ and a ground reference. This prevents the voltage at the base of the transistor Q₂ from being a "floating" voltage. Likewise, another filter circuit of the present invention teaches coupling a diode connected transistor Q₃ between the base of the transistor Q₂ and the ground reference. That is, the emitter of the transistor Q₃ is coupled to the base of the transistor Q₂ and the base and the collector of the transistor Q₃ are coupled to the ground reference.

Yet another embodiment of the present invention teaches an integrated circuit package having primary circuitry, an ESD protection device, a filter

circuit, and a conductive lead arranged to form a conductive path from a point external to the integrated circuit package to a point internal to the integrated circuit package. The ESD device, coupled in series between the conductive lead and a ground reference, is operable to limit the voltage magnitude of a transient electrical pulse occurring upon the conductive lead. The filter circuit, having an input electrically coupled to the conductive lead and an output electrically coupled to the primary integrated circuit, is operable such that the voltage magnitude of an electrical signal generated at the filter circuit output in response to the certain transient electrical pulse is less than the voltage magnitude of the certain transient electrical pulse itself.

Brief Description of the Drawings

Figure 1 is a schematic modeling an integrated circuit of the prior art.

Figure 2 is a schematic of an integrated circuit including a filter circuit in accordance with one embodiment of the present invention

5 Figure 3 is a schematic of an integrated circuit including a filter circuit in accordance with another embodiment of the present invention.

Figure 4 is a time plot of a voltage V_+ resulting from an ESD event voltage V_{ESD} dissipated by a standard ESD device.

10 Figure 5 is a time plot of a filtered voltage V_{F+} resulting from the filter circuit of the present invention operating upon the voltage V_+ of Figure 4.

Figure 6 is a schematic of a second filter circuit in accordance with another embodiment of the present invention.

15 Figure 7 is a schematic of an integrated circuit in accordance with yet another embodiment of the present invention, the integrated circuit including the second filter circuit of Figure 6 and post-package trimming circuitry.

Best Modes for Carrying out the Invention

With reference to Figure 2, an integrated circuit 100 in accordance with one embodiment of the present invention will now be described. The integrated circuit 100 includes primary circuitry 12, an electrostatic discharge (ESD) protection device 14, a terminal 16, and a filter circuit 102. The ESD protection device 14 is connected in series between the terminal 16 and a common ground reference 20 and serves to limit the voltage V_+ generated by a transient electrical pulse. The filter circuit 102 is connected in series between the terminal 16 and the primary circuitry 12.

The filter circuit 102 is designed to filter the voltage V_+ such that the primary circuitry 12 is protected from the full magnitude of the voltage V_+ . Therefore, while a voltage V_+ is present at the terminal 16, which is coupled to the ESD protection device 14, the input to the primary circuitry 12 is a filtered voltage V_{F+} generated by the filter circuit 12. Two preferred embodiments of the filter circuit 102 are described in more detail below with reference to Figures 3-7.

Turning next to Figure 3, a filter circuit 102 in accordance with one particular embodiment of the present invention will now be described. Figure 3 is a schematic of an integrated circuit 100 including primary circuitry 12, an ESD protection device 14, a terminal 16, and the filter circuit 102. The filter circuit 102 is connected in series between the terminal 16 and the primary circuitry 12. Therefore, while a voltage V_+ is present at the terminal 16, which is coupled to the ESD protection device 14, the input to the primary circuitry 12 is a filtered voltage V_{F+} generated by the filter circuit 12.

The filter circuit 102 includes two resistors R_1 and R_2 , two capacitors C_1 and C_2 , and two npn transistors Q_1 and Q_2 . The resistor R_1 has terminals 110 and 112 and the resistor R_2 has terminals 120 and 122. The capacitor C_1 has terminals 130 and 132 and the capacitor C_2 has terminals 140 and 142. The

5

transistor Q_1 has a base 150, a collector 152, and an emitter 154. The transistor Q_2 has a base 160, a collector 162, and an emitter 164. As will be appreciated, transistors such as Q_1 and Q_2 operate such that a voltage differential between the base and the emitter controls a current flow through the collector and emitter.

10

The components of the filter circuit 102 are connected as follows. The terminal 110 of the resistor R_1 , the terminal 120 of the resistor R_2 , and the collector 152 of the transistor Q_1 are electrically coupled together forming an input node 114 of the filter circuit 102. The terminal 140 of the capacitor C_1 is electrically coupled to the terminal 112 of the resistor R_1 and the terminal 142 of the capacitor C_1 is electrically coupled to the base 160 of the transistor Q_2 . The terminal 122 of the resistor R_1 , the collector 162 of the transistor Q_2 , the terminal 130 of the capacitor C_1 , and the base 150 of the transistor Q_1 are electrically coupled. The emitter 164 of the transistor Q_2 and the terminal 132 of the capacitor C_1 are electrically coupled to the common ground reference 20. The emitter 154 of the transistor Q_1 acts as an output of the filter circuit 102 that is electrically coupled to the input of the primary circuitry 12.

As described above with reference to Figure 1, when an ESD event occurs, the ESD protection device 14 limits the voltage V_+ to around, e.g., 50 Volts amplitude and less than 300 nanoseconds in duration. This voltage pulse is practically a "square wave," typically having steep rise and fall edges. For example, the rise and fall times may both be 10 nanoseconds or less. The following description of the operation of the filter circuit 102 is a response to such an ESD event.

Initially, both capacitors C_1 and C_2 are discharged and transistors Q_1 and Q_2 are off (*i.e.*, no current is flowing therethrough). On the rising edge of the V_+ pulse, the capacitor C_1 is charged according to the time constant $t_1 = R_1 * C_1$. Simultaneously, the transistor Q_1 turns on due to the voltage transmitted

through the capacitor C_2 with a dV/dt ramp rate at the base of the transistor Q_2 . The transistor Q_2 is preferably chosen such that its turn on time is short relative to t_1 so that the voltage across the charging capacitor C_1 is still at a low level when the transistor Q_2 turns on. When the transistor Q_2 turns on, current flowing across the collector 162/emitter 164 junction serves to discharge the capacitor C_1 and the voltage V_{F+} will drop to a low level.

While the preceding was occurring, the initially discharged capacitor C_2 has been charging due to the resistor R_2 and the input resistance present at the base 160 of the transistor Q_2 . The time constant $t_2 = C_2 * (R_1 + \text{base resistance})$ determines the time ($3*t_2$) when the transistor Q_2 will begin turning off. Preferably, a sufficiently lengthy time constant t_2 is selected in order to keep Q_2 saturated until the V_+ input pulse ends.

As the transistor Q_2 comes out of saturation, the capacitor C_1 begins charging (again) through the resistor R_1 . Then, on the falling edge of the pulse V_+ , the voltage V_{F+} rises momentarily as the capacitors C_1 and C_2 fully discharge.

Designing for a "worst case" scenario upon an integrated circuit might entail dealing with an ESD event resulting in a transient pulse voltage V_+ of about 50 Volts with a duration of about 300 nanoseconds. As will be appreciated, larger capacitive values will provide greater protection. Certain embodiments of the present invention are contemplated as integral to the integrated circuit thus making physical dimensions a limiting factor.

Under these circumstances, suitable values for the components are as follows. The capacitor C_1 may be between about 2 picofards and 25 picofarads. More preferably, the capacitor C_1 is about 15 picofarads. The resistor R_1 may be between about 500 ohms and about 10 Kilo ohms. More preferably, the resistor R_1 is about 2 Kilo ohms. The time constant t_1 should be greater than or equal to about 30 nanoseconds. The capacitor C_2 may be between about 5

picofards and 20 picofarads. More preferably, the capacitor C_2 is about 8.6 picofarads. The resistor R_2 may be between about 1 Kilo ohm and 20 Kilo ohms. More preferably, the resistor R_2 is about 5 kilo ohms. Preferably the time constant t_2 is greater than 100 nanoseconds. The resultant voltage curves 5 are shown in Figures 4 and 5.

Figures 4 and 5 plot a hypothetical voltage V_{ESD} and a resultant voltage V_{F+} , respectively, as functions of time. Note how the filtered voltage V_{F+} has 10 two spikes 200 and 202. The voltage spike 200 peaks at about 3 Volts while the voltage spike 202 peaks at about 1 Volt. In contrast with the 50 Volt pulse of V_+ , the voltage spikes 200 and 202 are much less likely to cause damage on subsequent circuitry.

Turning next to Figure 6, a filter circuit 300 in accordance with another embodiment of the present invention will now be described. As will be appreciated, the transistor Q_2 in filter circuit 102 of Figure 3 is controlled by a floating voltage applied at its base 160. The filter circuit 300 has filter circuitry 15 similar to filter circuit 102 but further includes a diode connected transistor Q_3 and a resistor R_3 which as connected provide a coupling to the common ground reference 20. The transistor Q_3 and resistor R_3 provide protection to the transistor Q_2 , particularly during transition periods when the voltage at the base 20 160 may go negative.

The resistor R_3 has terminals 310 and 312. Values ranging between about 20 Kilo ohms and 200 Kilo ohms are suitable for the resistor R_3 . The transistor Q_3 has a base 320, a collector 322, and an emitter 324. The emitter 25 324 of the transistor Q_3 and the terminal 310 of the resistor R_3 are electrically coupled to the base 160 of the transistor Q_2 . The base 320 and the collector 322 of the transistor Q_3 and the terminal 312 of the resistor 312 are electrically coupled to the common ground reference 20.

Thus when the voltage driving the base 160 of transistor Q_2 is negative, the transistor Q_3 will conduct a current limited by the resistor R_2 and prevent the base-emitter junction of Q_2 from voltage breakdown. Further, by coupling the base 160 of transistor Q_2 to the ground connected R_3 , the base 160 is no longer floating.

Figure 7 illustrates the use of the filter circuit 300 of Figure 6 with primary circuit 12 having a post-package trim circuit 400. In this embodiment, the post-package trim circuit 400 includes a fuse control logic device 402, a plurality of control wires G_1 through G_N , a plurality of PMOS transistors, and a plurality of thin film fuses having resistance values of R_{f1} through R_{fn} .

As will be appreciated, the logic device 402 is operable to blow the fuses in order to adjust (i.e. trim) an output voltage of the primary circuit 12 even after the integrated circuit has been completely packaged. However, these fuses are extremely sensitive so that even the attenuated voltage pulse generated by an ESD event with the standard ESD protection devices can blow these fuses causing irreversible damage to the integrated circuit. But, the filtered voltage V_{F+} produced when the filter circuit 300 is present is substantially smaller than V_+ and thus decreases the risk of damage to the post-package trim circuitry.

Although only a few embodiments of the present invention have been described in detail, it should be understood that the present invention may be embodied in many other specific forms without departing from the spirit or scope of the invention. While Figures 3 and 6-7 utilized the symbol normally associated with npn type transistors, the present invention contemplates embodiments utilizing other types of switches. By way of example, n-channel field effect transistors and even bi-polar transistors are suitable equivalents for the illustrated npn transistors. As will further be appreciated, the filter circuits of the present invention can be implemented with pnp transistors.

Therefore, the present examples and embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope of the appended claims.

Claims

I claim

1. A filter circuit suitable for protecting primary circuitry from transient electrical pulses, the filter circuit comprising:

5 two resistors R1 and R2 each having first and second terminals;

two capacitors C1 and C2 each having first and second terminals;

a transistor Q1 having a base, a collector and an emitter, wherein voltage applied to the base of the transistor Q1 can control a flow of current through the transistor Q1 between the collector and the emitter of the transistor Q1;

10 a transistor Q2 having a base, a collector and an emitter, wherein voltage applied to the base of the transistor Q2 can control a flow of current through the transistor Q2 between the collector and the emitter of the transistor Q2, the emitter of the transistor Q2 being an output of the filter circuit; and

wherein:

15 the first terminals of resistors R1 and R2 and the collector of transistor Q1 are electrically coupled, such electrical coupling being an input to the filter circuit;

the second terminal of the resistor R2 and the first terminal of the capacitor C2 are electrically coupled;

20 the second terminal of the capacitor C2 and the base of the transistor Q2 are electrically coupled;

the second terminal of the resistor R1, the collector of the transistor Q2, the first terminal of the capacitor C1, and the base of the transistor Q1 are electrically coupled; and

25 the emitter of the transistor Q2 and the second terminal of the capacitor C1 are electrically coupled to a common ground reference to which the primary circuitry is also coupled,

whereby a transient voltage pulse applied at the input of the filter circuit is filtered such that a voltage measured at the output of the filter circuit due to the transient voltage pulse is substantially less than the transient voltage pulse.

5 2. A filter circuit as recited in claim 1 wherein transistors Q1 and Q2 are npn transistors.

10 3. A filter circuit as recited in claim 1 wherein transistors Q1 and Q2 are n-channel field effect transistors.

15 4. A filter circuit as recited in claim 1 wherein transistors Q1 and Q2 are pnp transistors.

20 5. A filter circuit as recited in claim 1 further comprising:
15 a resistor R3 having first and second terminals;
a transistor Q3 having a base, a collector and an emitter, wherein voltage applied to the base of the transistor Q3 can control a flow of current through the transistor Q3 between the collector and the emitter of the transistor Q3; and
wherein:

25 the first terminal of the resistor R3 and the emitter of the transistor Q3 are electrically coupled to the second terminal of the capacitor C2; and

the base and the collector of the transistor Q3, the second terminal of the resistor R3, the emitter of the transistor Q2, and the second terminal of the capacitor C1 are all electrically coupled to a common ground reference.

6. A filter circuit as recited in claim 5 wherein the transistor Q3 is an npn transistor.

5 7. A filter circuit as recited in claim 5 wherein the transistor Q3 is an n-channel field effect transistor.

8. A filter circuit as recited in claim 1 wherein the filter circuit integral to an integrated circuit package.

10 9. A filter circuit as recited in claim 8 wherein the integrated circuit package further includes an electrostatic discharge (ESD) protection device and a primary circuit, an input of the ESD protection device and the input of the filter circuit being electrically coupled, and the output of the filter circuit and an input of the primary circuit being electrically coupled, whereby the ESD protection device and the filter circuit work together to protect the primary circuit from transient voltage pulses.

20 10. A filter circuit as recited in claim 1 wherein the filter circuit is suitable for protecting primary circuitry from electrostatic discharge events that are shorter than 300 nanoseconds, the value of resistor R₁ being between about 500 ohms and 10 Kilo ohms, the value of the resistor R2 being between about 1 Kilo ohm and 20 Kilo ohms, the value of the capacitor C1 being between about 2 picofarads and 25 picofarads, and the value of the capacitor C2 being between about 5 picofarads and 20 picofarads.

25 11. A filter circuit as recited in claim 1 wherein the value of the resistor R1 being about 2 Kilo ohms, the value of the resistor R2 being about 5

Kilo ohms, the value of the capacitor C1 being about 15 picofarads, and the value of the capacitor C2 being about 8.6 picofarads.

5 12. A filter circuit as recited in claim 1 wherein the turn-on time of the transistor Q₂ is less than the time constant R₁ multiplied by C₁.

10 13. A filter circuit as recited in claim 1 wherein the time constant R₂ multiplied by C₂ is large enough to render and maintain Q₂ saturated through a transient voltage pulses greater than 50 Volts and having a duration greater than 200 nanoseconds.

14. A filter circuit suitable for protecting primary circuitry from transient electrical pulses, the filter circuit comprising:

15 three resistors R₁, R₂ and R₃ each having first and second terminals; two capacitors C₁ and C₂ each having first and second terminals;

a transistor Q₁ having a base, a collector and an emitter, wherein voltage applied to the base of the transistor Q₁ can control a flow of current through the transistor Q₁ between the collector and the emitter of the transistor Q₁;

20 a transistor Q₂ having a base, a collector and an emitter, wherein voltage applied to the base of the transistor Q₂ can control a flow of current through the transistor Q₂ between the collector and the emitter of the transistor Q₂, the emitter of the transistor Q₂ being an output of the filter circuit; and

wherein:

25 the first terminals of resistors R₁ and R₂ and the collector of transistor Q₁ are electrically coupled, such electrical coupling being an input to the filter circuit;

the second terminal of the resistor R₂ and the first terminal of the capacitor C₂ are electrically coupled;

the second terminal of the capacitor C2, the base of the transistor Q2, and the first terminal of the resistor R₃ are electrically coupled;

5 the second terminal of the resistor R1, the collector of the transistor Q2, the first terminal of the capacitor C1, and the base of the transistor Q1 are electrically coupled;

the emitter of the transistor Q2 and the second terminal of the capacitor C1 are electrically coupled to ; and

10 the second terminal of the resistor R₃ is electrically coupled to a ground reference,

15 whereby a transient voltage pulse applied at the input of the filter circuit is filtered such that a voltage measured at the output of the filter circuit due to the transient voltage pulse is substantially less than the transient voltage pulse.

15. A filter circuit as recited in claim 14 wherein the transistors Q₁ and Q₂ are npn transistors.

16. A filter circuit as recited in claim 14 wherein the transistors Q₁ and Q₂ are n-channel field effect transistors.

20 17. A filter circuit as recited in claim 14 wherein the transistors Q₁ and Q₂ are pnp transistors.

25 18. A filter circuit as recited in claim 14 wherein the filter circuit is integral to an integrated circuit package.

19. A filter circuit as recited in claim 18 wherein the integrated circuit package further includes an electrostatic discharge (ESD) protection device and a primary circuit, an input of the ESD protection device and the input of the

filter circuit being electrically coupled, and the output of the filter circuit and an input of the primary circuit being electrically coupled, whereby the ESD protection device and the filter circuit work together to protect the primary circuit from transient voltage pulses.

5

20. An integrated circuit package comprising:

a conductive lead arranged to provide an electrically conductive path from a first point external to the integrated circuit package to a second point internal to the integrated circuit package;

10 an electrostatic discharge (ESD) protection device coupled in series between the conductive lead and a ground reference, the ESD device operable to limit the voltage magnitude of a transient electrical pulse occurring upon the conductive lead;

15 a primary circuit integral to the integrated circuit package; and

20 a filter circuit having an input and an output, the filter circuit input being electrically coupled to the conductive lead and the filter circuit output being electrically coupled to the primary integrated circuit, the filter circuit operable such that the voltage magnitude of an electrical signal generated at the filter circuit output in response to the certain transient electrical pulse is less than the voltage magnitude of the certain transient electrical pulse,

whereby the primary circuit is provided protection from the transient electrical pulse.

25 21. An integrated circuit package as recited in claim 20 wherein the ESD device is an RC filter.

22. An integrated circuit package as recited in claim 20 wherein the filter circuit includes the following:

two resistors R1 and R2 each having first and second terminals;
two capacitors C1 and C2 each having first and second terminals;
a transistor Q1 having a base, a collector and an emitter, wherein voltage applied to the base of the transistor Q1 can control a flow of current through the
5 transistor Q1 between the collector and the emitter of the transistor Q1;

a transistor Q2 having a base, a collector and an emitter, wherein voltage applied to the base of the transistor Q2 can control a flow of current through the transistor Q2 between the collector and the emitter of the transistor Q2, the emitter of the transistor Q2 being the filter circuit output; and

10 wherein:

the first terminals of resistors R1 and R2 and the collector of transistor Q1 are electrically coupled, such electrical coupling being the filter circuit input;

15 the second terminal of the resistor R2 and the first terminal of the capacitor C2 are electrically coupled;

the second terminal of the capacitor C2 and the base of the
15 transistor Q2 are electrically coupled;

20 the second terminal of the resistor R1, the collector of the transistor Q2, the first terminal of the capacitor C1, and the base of the transistor Q1 are electrically coupled; and

the emitter of the transistor Q2 and the second terminal of the capacitor C1 are electrically coupled.

25 23. An integrated circuit package as recited in claim 22 wherein the transistors Q₁ and Q₂ are npn transistors.

24. An integrated circuit package as recited in claim 22 wherein the transistors Q₁ and Q₂ are n-channel field effect transistors.

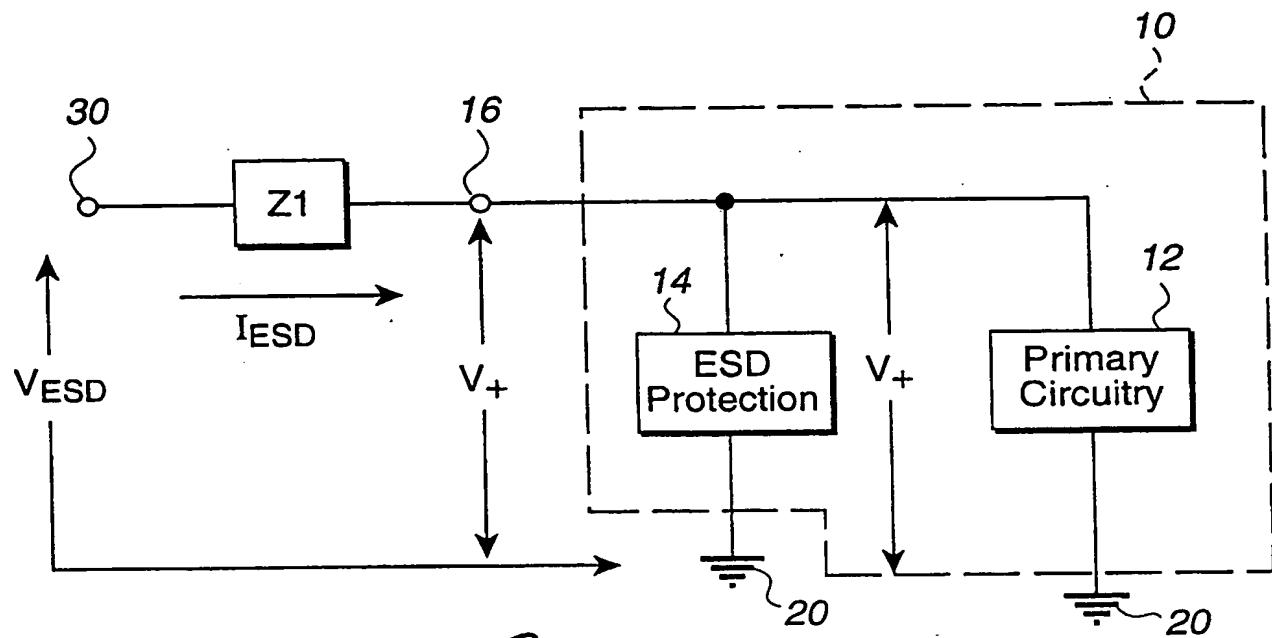
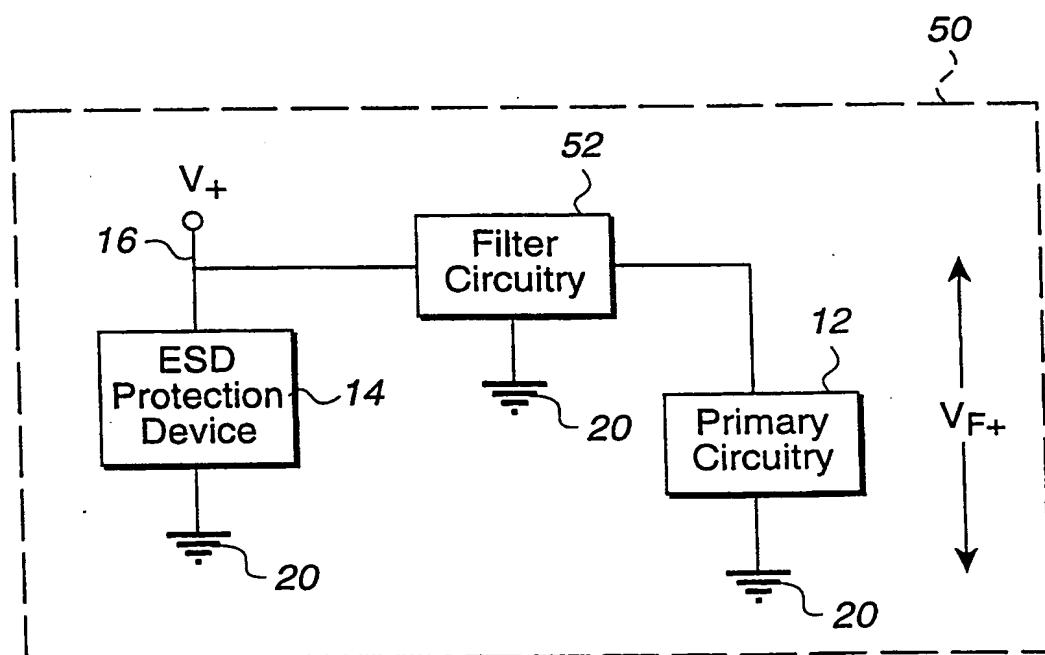
25. An integrated circuit package as recited in claim 22 further including a resistor R_3 having first and second terminals, the first terminal of the resistor R_3 and the base of the transistor Q_2 being electrically coupled, and
5 the second terminal of the resistor R_3 electrically coupled to the ground reference.

26. An integrated circuit package as recited in claim 25 further including a transistor Q_3 having a base, an emitter, and a collector, the base and
10 the collector of the transistor Q_3 being electrically coupled to the ground reference, and the emitter of the transistor Q_3 being electrically coupled to the first terminal of the resistor R_3 .

27. An integrated circuit package as recited in claim 20 wherein the
15 primary circuitry includes post-package trimming circuitry.

28. An integrated circuit package as recited in claim 27 wherein the post-package trimming circuitry includes a plurality of thin film fuses that may be selectively blown in order to alter the electrical characteristics of the
20 integrated circuit package.

1 / 5

*Fig. 1 (Prior Art)**Fig. 2*

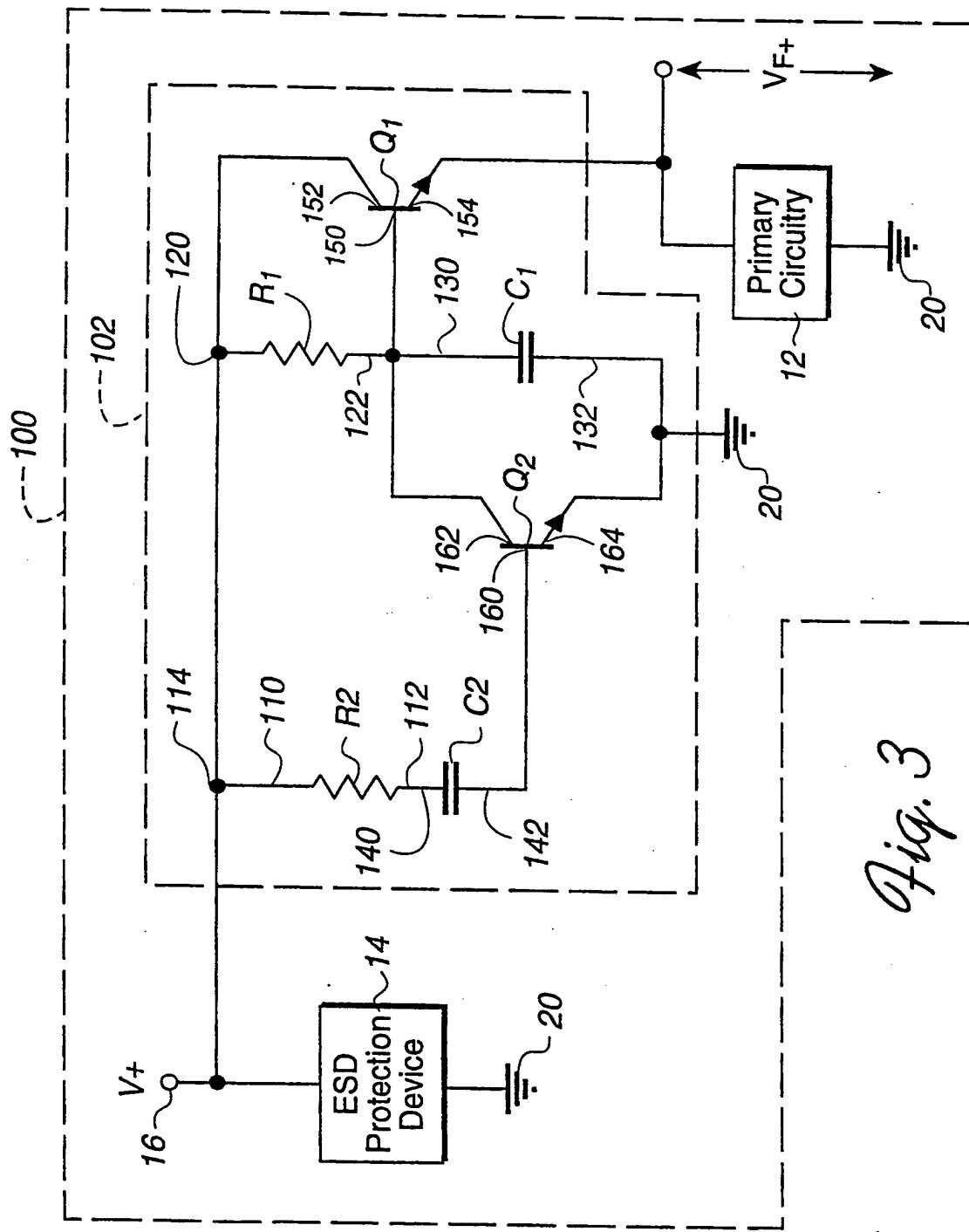


Fig. 3

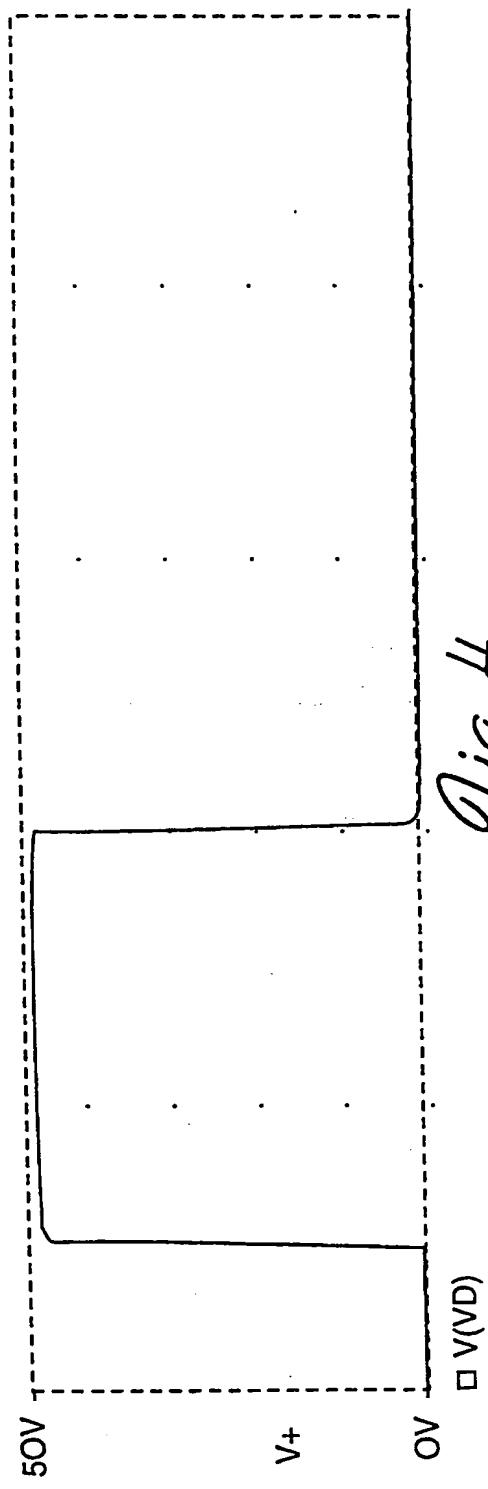


Fig. 4

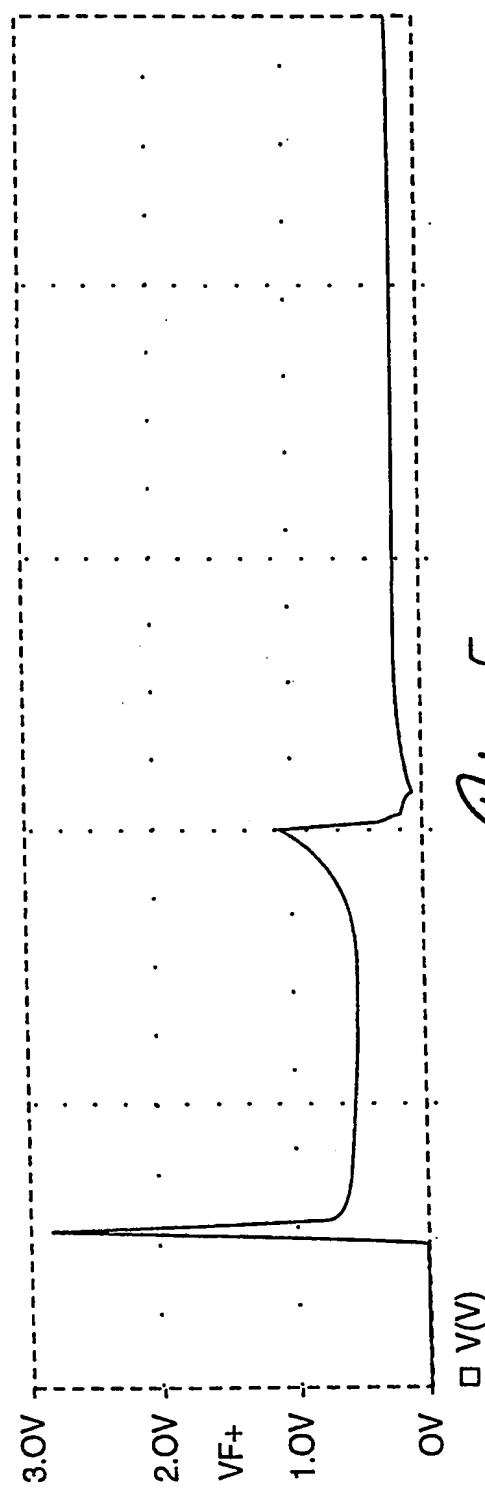


Fig. 5

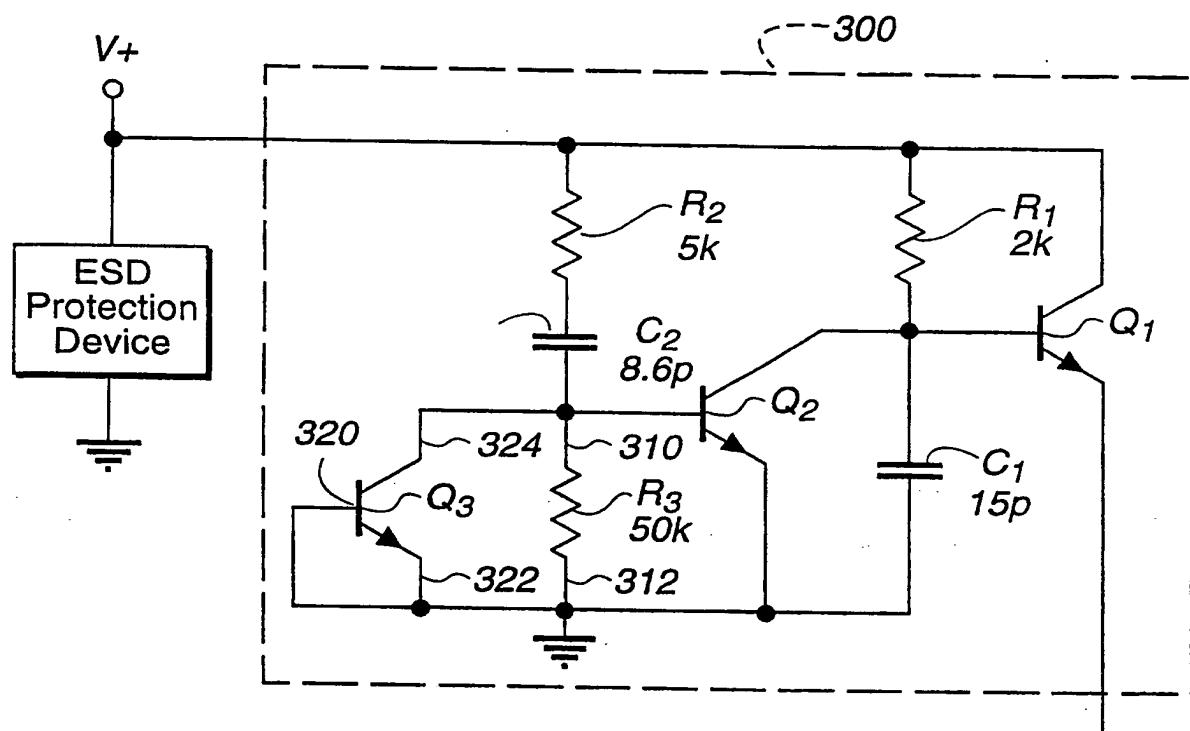
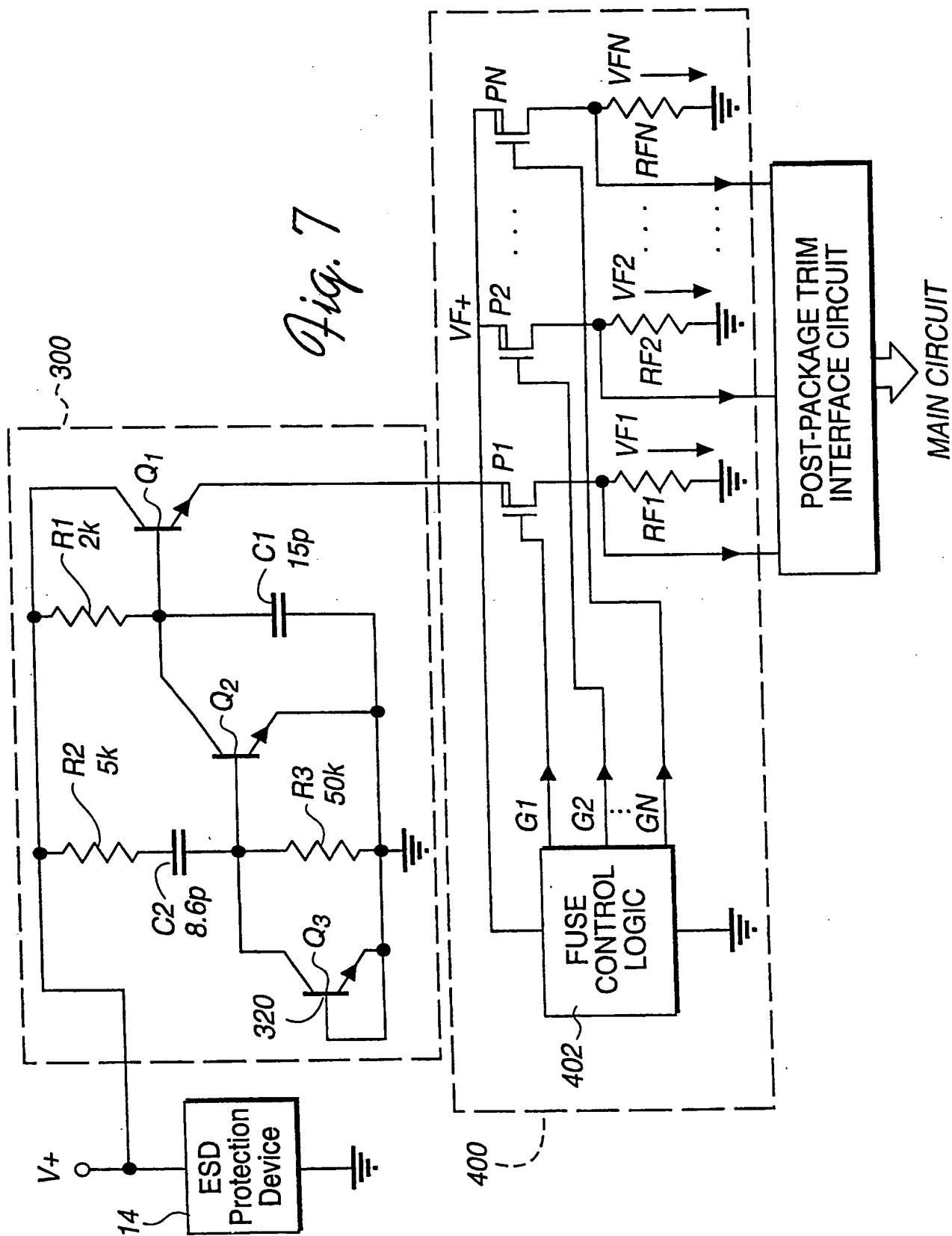


Fig. 6

5 / 5



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US99/00429

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :HO3K 5/08

US CL :327/327, 310, 313, 546

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 327/309, 310, 311, 313, 327, 545, 546; 323/901, 908; 361/13; 363/49, 50

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

search terms: esd or ((electro(w)static or electrostatic)(w)discharge), filter, soft power switch

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category ^a	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,587,685 A (JOHANSSON) 24 December 1996 (24/12/96), see Fig. 2.	1-28
X	US 5,440,162 A (WORLEY et al) 08 August 1995 (08/08/95), see Fig. 4.	20, 21 27 and 28
A	US 5,155,648 A (GAUTHIER) 12 October 1992 (12/10/92), see Fig. 2.	1-28
A	US 4,900,951 A (SAITO et al) 13 February 1990 (13/02/90), see Fig. 2.	1-28

Further documents are listed in the continuation of Box C.

See patent family annex.

"	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, and the combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

10 MARCH 1999

Date of mailing of the international search report

26 MAR 1999

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Facsimile No. (703) 305-3230

Authorized officer

TERRY D. CUNNINGHAM *[Signature]*

Telephone No. (703) 308-4876